THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 29

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KIM MEINERTH, JOHN KIRK, and GEORGE LORD

Appeal No. 1997-4350
Application No. 08/574,848[1]

ON BRIEF

Before KRASS, BARRETT, and DIXON, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 4 and 5, the only claims pending in the application.

[1] Application for patent filed December 19, 1995. According to the appellants, this application is a continuation of Application No. 07/748,358, filed August 21, 1991, now abandoned.

The invention is directed to a computer system employing a duplicate tag store having duplicates of the main memory addresses contained in a CPU cache tag store. The invention is said to minimize traffic on the system bus and the CPU bus by eliminating bus transactions for memory requests to memory locations not present in the duplicate cache store. A bus transaction is generated only for memory requests to locations present in the duplicate tag store.

Independent claim 4 is reproduced as follows:

4. A computer system comprising:

a main memory having memory locations identified by main memory addresses;

a processor unit, coupled to the main memory, including

a CPU for processing data stored in the memory locations;

a CPU cache memory for storing the processed data; and

a CPU cache tag store containing the main memory addresses of the processed data stored in the CPU cache memory;

an input/output bus, coupled to the processor unit;

a plurality of input/output devices connected to the input/output bus for issuing memory requests containing main memory addresses;

a duplicate tag store, coupled directly to the input/output bus, having duplicates of the main memory addresses contained in the CPU cache tag store;

means for comparing an address in one of the memory requests with the addresses in the duplicate tag store; and

means, responsive to an address in said one of the memory requests matching an address in the duplicate tag store, for issuing an invalidate request to ensure that the most current value of the data is accessed.

The examiner relies on the following references:

Hartwell et al. (Hartwell)	4,858,234	Aug. 15, 1989
Milia et al. (Milia)	5,226,146	Jul. 6, 1993
	(effective filing date Oct. 28, 1988)	

Claims 4 and 5 stand rejected under 35 U.S.C. 103 as unpatentable over Milia in view of Hartwell.

Reference is made to the brief and answer for the respective positions of appellants and the examiner.

OPINION

We reverse.

Independent claim 4 requires, *inter alia*, that there be "a duplicate tag store, *coupled directly to the input/output bus*, having duplicates of the main memory addresses contained in the CPU cache tag store" [emphasis ours].

The examiner applies Milia to claim 4, identifying elements of Milia as corresponding to various claimed elements, as set forth at page 3 of the answer. The examiner notes that Milia does not explicitly teach the data processing system comprising a CPU for processing data, a duplicate tag store connected to the I/O bus, and a plurality of I/O devices. The examiner contends that it would have been obvious that the data processing system of Milia does comprise a CPU "in order to function properly" and an I/O bus in order to connect all I/O devices such as a keyboard, a mouse, a printer, etc. because these components are basic to conventional data processing systems. We agree with this much of the examiner's analysis.

However, the examiner then relies on Hartwell for the teaching of connecting an I/O unit directly to a system bus

and/or an I/O bus and concludes that it would have been obvious to combine the teachings of Milia and Hartwell "*in order to achieve a more flexible and higher bus performance computer data processing system because to connect a device from one bus connection to another increase* [sic] *the flexibility to the computer system architecture and avoid introduces* [sic] *complexities in the system*" [answer, page 4, emphasis in the original].

It is our view that the examiner has failed to establish a prima facie case of obviousness with regard to the claimed subject matter. We do not find the examiner's rather trite recitations of "more flexible," "higher bus performance," and "increase the flexibility," per se, to constitute a cogent rationale as to why the skilled artisan would have been led to place the duplicate cache tag store of Milia on the I/O bus. It is true that the artisan would like increased flexibility and higher bus performance but the examiner has presented no evidence, and we are aware of no evidence, other than appellants' own disclosure, which would have led the skilled

artisan to recognize that more "flexibility" and "higher bus performance" would ensue if the duplicate cache tag store of Milia would be connected directly to the I/O bus. It is only appellants' disclosure which teaches the advantages, viz., minimized traffic on the system bus and the CPU bus, achieved by connecting the duplicate cache tag store directly to the I/O bus. Thus, in our view, even if a duplicate cache tag store could be considered an I/O unit, it would not have been obvious, within the meaning of 35 U.S.C. 103, to have placed the duplicate cache tag store of Milia directly on the I/O bus (rather than on the system bus as taught by Milia), merely because Hartwell shows an I/O unit connected directly to an I/O bus, without some suggestion for doing so.

Moreover, the examiner's reasoning is faulty because, as argued by appellants, a duplicate cache tag store is, in fact, *not* an I/O unit. An I/O unit is an element which inputs or outputs data, such as a disk storage device, a printer, a keyboard, a mouse, etc. A duplicate cache tag store is not such a device for inputting or outputting data. Therefore, without the hindsight gleaned from appellants' disclosure,

there would have been no reason for the artisan to have directly connected the duplicate cache tag store of Milia to the I/O bus and the mere suggestion by Hartwell of placing an I/O unit directly on an I/O bus, which is where one would expect to find such I/O units, would not, in any way, have led the artisan to connect Milia's duplicate cache tag store, which is, decidedly, not an I/O unit, directly to the I/O bus.

The examiner's decision rejecting claims 4 and 5 under 35 U.S.C. 103 is reversed.

REVERSED

ERROL A. KRASS Administrative Patent Judge	)
LEE E. BARRETT Administrative Patent Judge	) BOARD OF PATENT APPEALS AND INTERFERENCES
JOSEPH L. DIXON Administrative Patent Judge	)

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